

Guillermo Alonzo Vera Rojas

141 Columbia Dr. SE. apt. 20.
Albuquerque NM 87106

Telephone (505) 720-4633
Email: alonzo@ece.unm.edu

Objectives

To obtain a PhD Degree developing novel reconfigurable logic architectures for signal processing applications.

Education

- 08/03 PhD Candidate – Electrical Engineering Department
University of New Mexico
- 05/04 MsC in Electrical Engineering
University of New Mexico
- 12/98 BSc. in Electrical Engineering
Catholic University of Peru
Thesis: Encryption System Design Implemented on Programmable Logical Devices (CPLDs).

Professional Experience

- 09/04-12/06 **Research Assistant**
Air Force Research Labs & UNM. Single Event Upsets (SEUs) emulation and mitigation techniques for space-borne FPGA-based digital systems.
- 05/06-08/06 **Internship Los Alamos National Laboratory**
T-7 Mathematical Modeling and Analysis Group
Analysis, development and implementation of Basis Pursuit principle for signal denoising and inverse problems.
- 09/03-08/04 **Research Assistant**
Xilinx University Program & UNM. Embedded systems tutorials for undergraduate and graduate students, using Xilinx's EDK tool. Maintainer of program website.
- 06/03-08/03 **Instructor**
University of New Mexico - Introduction to Computer Architecture (EECE337)
Main topics are Memory design considerations, Computer Arithmetic and instruction sets, CPU structure & function, instruction-level parallelism and Superscalar processors, Control Unit Operations and microprogramming.
- 01/03-08/03 **Graduate Mentor**
PURSUE-NASA Lab - Integration of CPLD in Lobot Jr. Design.
Goal of the project is a redesign of the whole system to generate a new generation of Lobot Jr. adding flexibility, low power capabilities and scalability by incorporating CPLD technology.
- 09/02-12/02 **Consultant**
Kestrel Corporation
FPGA Approach to Real Time Registration of Medical Images
- 08/01-08/02 **Consultant**
PricewaterhouseCoopers (Lima – Peru)
Consultant and security auditor on information systems and networks, acting as part of a technical and manager team for several kinds of projects:
– Vulnerability assessment and Forensic analysis on Information systems.

- Data and information technology security reviews and consulting of effectiveness in Information Technology units.
- 04/01-08/02 **Invited Professor**
 Scientific University of Peru
 Information systems security (Course (4th year))
- 01/99-08/01 **Security Engineer**
 Cosapisoft S.A (Lima – Peru)
 Security information systems and networks, responsible and Project Manager for:
- TCP/IP network implementations on several financial and commercial institutions; Lima-Peru.
 - Design and implementation of security architecture and policies on several financial and commercial institutions, Lima, Peru.
 - Vulnerability Assessment and Intrusion Detection.
- 11/99-04/00 **Research Assistant**
 Digital Signal Processing Research Group (PUCP)
 Degree Work: Encryption System Design Implemented on Programmable Logical Devices. Excellent mention granted.
- 03/98-12/00 **Teaching Assistant**
 Catholic University of Peru, Courses:
- Analog Circuits (4th year)
 - Microelectronics Laboratory (5th year)

Publications

- A. Vera, Uwe Meyer-Baese and M. Pattichis “, An FPGA based rapid prototyping platform for wavelet coprocessors”; Independent Component Analyses, Wavelets, Unsupervised Smart Sensors, and Neural Networks Conference, SPIE2007.
- Uwe Meyer-Baese, A. Vera, A. Meyer-Baese, M. Pattichis and R. Perry“, Smart Altera Firmware for DSP with FPGAs”; Independent Component Analyses, Wavelets, Unsupervised Smart Sensors, and Neural Networks Conference, SPIE2007.
- Guillermo A. Vera, Jorge E. Parra, Craig Kiev, Marios Pattichis and Howard Pollard. “Integrating reconfigurable logic in the first digital logic course”; International Conference on Engineering Education, ICEE2006, July 2006, San Juan, Puerto Rico.
- Uwe Meyer-Baese, A. Vera, A. Meyer-Baese, M. Pattichis, R. Perry. “Discrete wavelets transform FPGA design using MatLab/Simulink”; Independent Component Analyses, Wavelets, Unsupervised Smart Sensors, and Neural Networks Conference, SPIE2006.
- Yan Wang; Benito, F.; Vera, G.A.; Jamshidi, M., "Control design for diagnostic and prognostic of hardware systems," Fuzzy Systems, 2004. Proceedings. 2004 IEEE International Conference on, vol.1, no. pp. 457- 462 vol.1, 25-29 July 2004
- Guillermo A. Vera, C. Kief, J. Parra and M. S. Pattichis. “Educational Uses of FPGAs”; IEEE Circuits and Devices Magazine, Sept/Oct 2004
- C. Kief, Guillermo A. Vera, J. Parra and M.S. Pattichis. “Board of Education - V1000 Prototyping Platform Development,” Xcell Journal, Issue 51, Winter 2004.
- Guillermo A. Vera, J. Parra, C. Kief, and M. S. Pattichis; “Educational Uses of FPGAs,” submitted to the Microelectronics Systems News website, July 2004
- Guillermo A. Vera, J. Sotelo. “Basic blocks for Analog Integrated Circuits Design”, IV Workshop IBERCHIP, Marzo 1998, Mar del Plata – Argentina.
- J. Sotelo and A. Vera. “CMOS Design of Analog Integrated Circuits”, Research project for Concytec (National Council of Science and Technology). Lima – Perú 1998.
- Guillermo A. Vera. “Design Considerations of Integrated Ladder Filters with Switched Capacitors”, Memorias, V Congreso Internacional de Ingeniería Electrónica, Eléctrica y Sistemas, Tacna-Perú, Pags. 35 - 41, Agosto 1998.

Talks

- Digital Signal Processing using FPGA: A crash course; presented at “Jornadas de sistemas de Telecomunicaciones”, Escuela Politecnica del Litoral, Guayaquil – Ecuador; January 2007.
- Digital Signal Processing using FPGA workshops; Pontificia Universidad Catolica del Peru, Lima – Peru; August 2006.
- v7.1 DSP Design Flow Workshop, presented at “Signal processing applications on FPGAs Workshop”; Universidad Javeriana – Cali, Colombia, September 2005.
- Digital Design with ISE and Programmable Logic with an introduction to the System Generator and the Embedded Development Kit, ISTEK XIV General Assembly, Tampa Florida, December 2004.
- Xilinx University Program, Programmable Logic, and the University of New Mexico, presented at the Pan-American Advanced Studies Institutes Program, Bolivia, June 2004.
- Defense methods and techniques against hacking. 3rd Anual Conference CETESIS – Herramientas de informacion una base para el cambio 6 – 21 October. Universidad Nacional Federico Villareal.
- Internet Security. Asociación de Estudiantes de Electrónica - AEE Conference. Sección de Electricidad y Electrónica. Catholic University of Peru

Short Courses

- 2005 Xilinx Customer Education: Advanced Embedded System Development.
- 2003 XUP – DSP Design Flow and FPGA Design Flow, University of New Mexico.

University Service

- President of the ECE - Graduate Students Association during the period 2004-2005.
- Directed teams to completely renovate lab manuals and materials for ECE238, Introduction to Digital Systems class. 2003-2006.
- Facilitator for Xilinx University Program (XUP) and UNM joint activities (professor’s workshops) and research projects. Maintainer of program website (www.eece.unm.edu/xup). 2003-2006

Computer skills

- Operating Systems: UNIX, Windows 2000/XP. Administrator and user level.
- Computers design tools: ISE 8.1, Pspice, Hspice, Tanner, Orcad, Tedmos, Eagle.
- Hardware description languages: VHDL, AHDL.
- Mathematical and simulation tools: ModelSim, Matlab, Khoros.
- Program Languages: C, Handel-C and Perl.

Language skills

- Spanish: Native speaker
- English: Fluent
- French: Intermediate

Key qualifications

Leadership, interpersonal skills. Ability to manage technical relationship with clients and partners. Research skills and experience in projects implementation and proposal support with several governmental, financial and commercial institutions.